CURRENT CONTROLLED CURRENT CONVEYOR & PHYSICAL CONSTRAINTS OF THE MOS - A POWER PERSPECTIVE

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Abstract

Tran conductance amplifier is a good addition to the Analog VLSI, but it fails to conceptually emulate an OPAMP. However, a current conveyor seems to be a promising device for Analog VLSI regime, to replace a traditional OPAMP. Among its various important characteristics, it has the capability that voltage on high impedance node can reflect on to its low impedance node to mimic the popular virtual short circuit of an OPAMP. A current feedback operational amplifier (CFOA) is also a choice for analog design, but the current conveyor is preferred as it is found more versatile than a CFOA.

Keywords: Amplifier, Translinear Loops.

CM TECHNIQUES AND DEVICES

Under Current Mode, usage of various techniques can be readily seen. These techniques are usually the outcomes of the processes or functions controlled or governed by the current signals instead of well established voltage signals. Current mirrors, translinear loops, source coupled differential pair amplifiers etc are the key building blocks of the CM systems. The switched current technique is also a current mode technique where current in a branch is switched. The Current Conveyor is considered as the next higher level CM Devices.

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CM techniques have some distinctive advantages. The do not need high gain and high performance amplifiers, no need to high precision components, can be realized fully by using transistors, their speed, bandwidth and accuracy is better than their VM counterparts, can realize each and every function realizable in VM and usually functional current can be scaled to any smaller magnitude.

CURRENT CONVEYORS

OPAMP is a VM device. It's natural characteristics (Zi=∞,Zo=0, AV=constant) enable cascading without degradation in performance, and the characteristics are determined solely by the external components. An ideal CM circuit is entirely different (Zo=∞,Zi=0, AI=constant). Current amplification of an ideal device is usually set to unity because it may otherwise result in large static power consumption. Current conveyor (CC) is the ideal CM device. The first generation and second generation current conveyors differ in the existence or non existence of current at high impedance input node y. The characteristics of the

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ideal 2nd generation current conveyors is given in Eq.

The general block diagram of a current conveyor is given below in Fig.

In Eq. '+' sign stands for the direction of current i_z same as shown, '−' stands for a reversed direction of i_z with respect to i_x , thus (CCII±). Node 'y' is the voltage controlled node with no current. The impedance looking into nodes 'x' is ideally zero. Node 'z' is the output node with infinite output impedance, i.e. $R_x = 0$, $R_z = \infty$. Further, voltage applied at node 'y' will appear at node 'x', current forced at node 'x' will be conveyed to node 'z'. The current i_x remain independent of voltages v_x .

FEATURES OF CURRENT CONVEYORS

The advantages and characteristic features of the use of CCII may be as follows:

Effort to Simulate Opamp: The CCII behaves more or less like an opamp, where the characteristics of the system comprising a CCII are determined solely by the external components and not the CCII used. **NTERCHANGEABLE Operation Mode:** A CCII can be used in both VM and CM applications with the peculiar feature that the system remains comparatively simpler.

Current Mirror: The basic constituent of the CCII is a current mirror. Therefore the design of a CCII is not as tedious as the design of an opamp, which needs highly sophisticated design skills.

Low Gain: A CCII does not need a high gain, therefore they do not need high performance amplifiers. This feature renders it a simple device to design and a simple device to use.

Simplicity of Design: A CCII does not need high precision components. They usually prefer comparative biasing signal levels. For example a reference current of 10μA changes to 11μA, it is not going to make any alteration in functionality of the current conveyor. However this 10% disturbance in biasing of a high performance voltage amplifier may cause an all over change in functionality of the amplifier. A CCII may be designed using transistors.

Application Simplicity: From application point of view, the use of a CCII is simpler. It can realize a negative resistance with utmost simplicity compared to the use of an opamp. The circuit that appears in [12] is based on careful utilization of positive feedback, and also uses three resistors with an opamp. The current conveyors have a broad spectrum of applications like amplifiers, converters, filters, switched current circuits, switched capacitor circuits, oscillators, negative impedance realization etc. a few to mention.

I/O IMPEDANCE: An ideal CCII has $R_o = \infty$ *and* $R_x = 0$, $R_y = \infty$. This helps in reducing the loading effects when the device is driving or being driven by other stages.

BANDWIDTH: of a CC is usually high because it has no global feedback. Feedback may be incorporated, but is usually of local nature. This leads to the increased bandwidth. Further, a CC is basically composed of current mirrors, and the current mirrors have CS and CG amplifier configurations. A CG (used for cascode) amplifier is free of miller effect.

Basic Considerations: The Current Mirror

A current mirror is an arrangement of transistors which produces reliable output current as a replica of the reference current in the circuit. A simple current mirror arrangement is shown in the Fig. below. Transistor M1 develops gate – source voltage that is used by the other transistor to generate a proportional copy of the reference current. Ideally, if the two transistors are maintained under identical conditions, the current in their drains will be in proportion of their aspects.

The basic of current mode circuits are the differential pair amplifier and current mirrors. Differential amplifier in itself a good idea, but needs gain boost for feedbacks, and also it has limited applications in CM signal processing. Current mirror is the bone of the CM signal processing. Some discussion regarding this block is considered here. An ideal mirror has some specific characteristics like input impedance output impedance $r_o = \infty$, current gain A_I = Aspect Ratio of the transistors, infinite Bandwidth, infinite Slew Rate, ON Time = 0, output current does not droop with load resistance, it can source output current at any voltage right from 0 to infinity etc. However, a real current mirror has its own limitations, and certain non- idealities. Its frequency response is given in the Eq. through. The factors that cause non idealities in a current mirror are as follows.

2nd GENERATION CURRENT CONTROLLED CURRENT CONVEYOR - CCCII

As far as the realization of current conveyors is concerned, there are various techniques which are used in the practice of designing the current conveyors. The method of using a translinear cell in the main cell along with a push pull stage as the output stage is considered to be the best. The push pull stage specifically enhances the current

handling capability of the conveyor side by side maintaining the high output impedance level.

In the past decade, the current conveyors have gone through several different stages. All these stages have their own merits and applications. The device which has attracted a fare share of the designers attention is the second generation current controlled current conveyor (CCCII). A CCCII is basically a current controlled CCII. In fact in CCII, there exists a non ideality of non zero 'X' node impedance. This impedance lacks a proper control and needs to be adjusted for a design along with a tradeoff between a lower parasitic impedance and other specifications, such as power consumption, linearity, dynamic range.

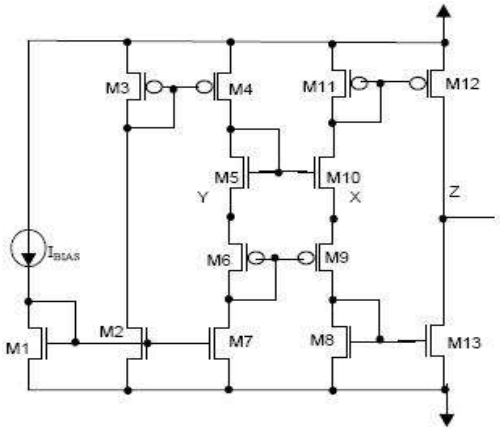

Figure: Translinear Circuit Schematic of the CCCII

Further in practical circuit applications, a CCII usually requires an external resistor to set different currents in the circuit. This is looked upon as limitation of a CCII. Thus if the resistance of node 'X' is made controllable and adjustable, then from the designers' point of view, it can be utilized for advantage. In fact, the node 'X' input resistance can be used as a circuit element and can help reducing the burden of ONE resistance per CCCII from the circuit. This can also lead to the resistance free design of some specific analog applications, as is demonstrated by the authors by realizing an oscillator with minimized use of passive components, and by realizing some other applications like resistance free phase shift oscillator and quadrature oscillator.

Design Approach Of The CCCII

CCII has been introduced earlier as a "natural" building block in analog circuit design. The enhancement type NMOS transistor can be regarded as a basic circuit that can realizes the CCII as shown in Fig. This not only gives the idea of the importance and usefulness of CCII, but also introduces a particular analogy between a MOSFET and a CCII.

The MOSFET works at $V_{GS} = V_X$, for a gate drive of (V_Y -V_{GS}), the channel current sets $I_Z = I_X$. the gate is treated as node *Y*, the node *Y* current is zero. The transconductance of the MOSFET relates the output current (I_Z) to the gate drive. Current at the node *X* is introduced by connecting a resistance at the source of the MOSFET. It is thus easy to perceive that the characteristic requirements of a CCII are fulfilled.

POWER CONSIDERATIONS

The semiconductor industry has experienced tremendous growth in the continuing past so that every aspect of the VLSI technology has experienced a phenomenal growth. The industry has now reached a critical point where there have arisen a number of challenges that threaten the continuation of advancement any further. *50nm* technology node is critical in this regard where from onwards, the technological challenges appear to be installing the growth any further unless an amendable solution is brought forth. They are the "Technology Challenge", the "Power Challenge", and the "Design Productivity Challenge". That is Lithography at and below 50nm, sub-microwatt power requirement at MIPS, and the design improvement at a rate of 50% per year or higher.

Heavy scaling has become a trend. The deep submicron technologies, from 130nm onwards, pose a new set of design problems. We can now implement tens of millions of gates on a reasonably small die, leading to a power density and total power dissipation that is at the limits of what packaging, cooling, and the other infrastructure can support. The leakage current is another problem increasing dramatically, to the point where, in some 65nm and lower designs, leakage current appear to be comparable with the dynamic current.

These changes are having a significant effect on how chips are designed. The power density of the highest performance chips has grown to the point where it is no longer possible to increase clock speed as technology shrinks. As a result, designers are designing multi-processor chips instead of chips with a single, ultra-high speed processor.

LV AND LP APPROACHES

In order to satisfy the needs of the electronic systems, comprehensive approaches are to be adopted which include the design at lower supply voltages, choose appropriate and power conscious architecture, suitable and appropriate circuit styles

in CMOS technology. Principles of low power design evolve as early as in 1960's. Meindl formulated some very basic rules for low power design

Some of these principles are like the following.

- Low Biasing Supply,
- Use Analog Circuits wherever possible,
- Use Smallest Geometry and Highest frequency transistors,
- Use Justifiably extra hardware wherever possible, design of multi stage amplifiers instead of single stage one, and,
- Use MOS/CMOS as a general VLSI design device.

ANTICIPATING SYSTEM LIMITS

It appears as if the future of Low Power VLSI (ULSI or GSI) will be governed by a hierarchy of theoretical and practical limits which can be classified as the following:

1. Fundamental Impositions

The fundamental impositions come from the basic physical principles of Thermodynamics, Quantum Mechanics and Electromagnetic. As the device size reduces, the effects concerning the above outlined principles become more and more pronounced. The frustrating performances exhibited by the nanometer devices is perhaps due to the reality that the ballistic transport is getting hard to establish.

2. Material Limits

The material limits are determined from carrier mobility, saturation of carrier velocity, breakdown of field strength, thermal conductivity and the relative dielectric constant of insulators for interconnects.

3. Device Limit

This refers to basically the minimum channel length of the MOSFETs, because the channel length directly determines the switching energy and the intrinsic delay. Response time is also affected by distributed RC network of the interconnect.

4. Circuit Level Limit

A logic is usually defined in terms voltage levels. Voltage magnitude is arbitrary, but there is a limit on scaling down the logic levels. For example, the logic restoration in static CMOS circuits requires a theoretical minimum supply voltage. This minimum supply voltage must satisfy the condition.

5. System Limits

The system limits is a complex phenomena. Besides the restrictions and considerations necessary for system design, a system depends upon all other restrictions as have been briefly discussed above. The specific considerations which impose a limit on the system are a)- chip architecture, b)- power delay product (PDP) of the CMOS and interconnects, c)- cooling capacity of the packaging technology d)- physical size of the chip and the e)- clock frequency and distribution [34,113]. A few important considerations are to be investigated as far as

6. Mosfet Sizing

Area on the wafer is one of the important physical entity. Appropriate sizing of the MOSFETs is a design aspect which determines how much the functionality could be afforded on the predetermined chip area, also and how it would perform. Larger sized MOSFETs occupy more area and contain larger capacitance and hence causes an increases in delay.

Conclusion

In this work several basic building blocks are designed. CMOS *inverter* shows 37% improvement in power with a minor performance sacrifice, CCCII designs are presented for 40µW – 300µW power range and are applied to different applications, a general purpose 3GHz VCO requires <125µW and the long range translinear multiplier needs <150µW. This work also addresses the innovative use of CCCII to the digital aplications. The CCCII have better current drive and therefore can eliminate the use of interface drivers. The present form of the CCC may not be justified on the area usage, but a suitable version of the CCC may be obtained to such applications. In present work, 1T model of the CCC is proposed. Simulation results suggest a whole improvement even compared to the standard CMOS realization in the same technology node. For example, Table 8.9 shows a reduction in power by half (6µW as compared to 10µW) and the delay by a factor of 20 (5ps as compared to 85ps).1T CCCII model suitably realizes polar XOR/XNOR and shows excellent performance.

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